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JIM WILLIAMS
PAPERS

High-speed data-conversion circuits

The variety of circuits that prove useful in high-speed data conversion is almost limitless. Here is a collection of circuits that can turn out to be lifesavers in several situations.

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Any reasonably complete listing of the types of circuits that you can use in data conversion and analog/digital data acquisition would be long indeed. Although books have been written just on D/A and A/D converters, such circuits are hardly the only ones that prove useful in acquiring fast-changing analog signals. You almost can't mention ADCs without also bringing up sample and hold (S/H) circuits. Voltage-to-frequency converters offer a very attractive alternative to more conventional ADCs, especially where you need signal isolation or outstanding linearity. Comparators are the heart of any analog-to-digital conversion scheme. Trigger circuits let you view and capture waveforms that recur at intervals that aren't perfectly periodic. Time-to-voltage converters let you see how pulse widths and time intervals vary as a function of time, and rms-to-dc converters extract an important property of ac signals—their heating value. There is a measure of commonality among the techniques you use to design such circuits. Here for your entertainment and edification is a potpourri of useful circuits that perform diverse functions.

In **Fig 1a**, the LT1016 comparator and the LT1122 high-speed FET amplifier combine to form a high-speed V/F converter. A variety of circuit techniques yields a 1-Hz to 10-MHz output. The circuit continues to function with a 20% overrange ($V_{IN} = 12V$; $f_{OUT} = 12$ MHz). This circuit has a wider dynamic range (140 dB, or seven decades) than any unit available commercially. The 10-MHz full-scale frequency is 10× as high as that of currently available monolithic V/F converters.

The theory of operation depends on the identity $Q = CV$. Each time the circuit produces an output pulse, it feeds back a fixed quantity of charge (Q) to a summing node (7). The circuit's input furnishes a comparison current at the summing node and a monitoring amplifier's feedback capacitor integrates the difference signal. The amplifier controls the circuit's output-pulse generator, completing a feedback loop around the integrating amplifier. To maintain the summing node at zero, the pulse generator runs at a frequency at which the pumped charge just offsets the current produced by the input signal. Thus, the output frequency is linearly proportional to the input voltage.

IC_1 is the integrating amplifier. Stabilizing IC_1 with IC_2, a chopper-stabilized op amp, produces 0.05 μV/°C of offset drift. IC_2 measures the dc value of the negative input, compares it with ground, and forces the positive input to maintain the offset balance in IC_1.

Note that IC_2 is an integrator that cannot see high-frequency signals. It functions only at dc and low frequencies.

Integrator IC_1 has a 68-pF feedback capacitor. When you apply a positive voltage to the input, IC_1's output integrates in a negative direction (**Fig 1b,** trace A). During this period, IC_5's inverting output is low. The paralleled HCMOS inverters form a reference-voltage switch. The LT1034s (driven by the LM134 current source and the Q_3/Q_4 combination) establish the reference voltage; a small input-voltage-related term adds to the reference, improving overall circuit linearity.

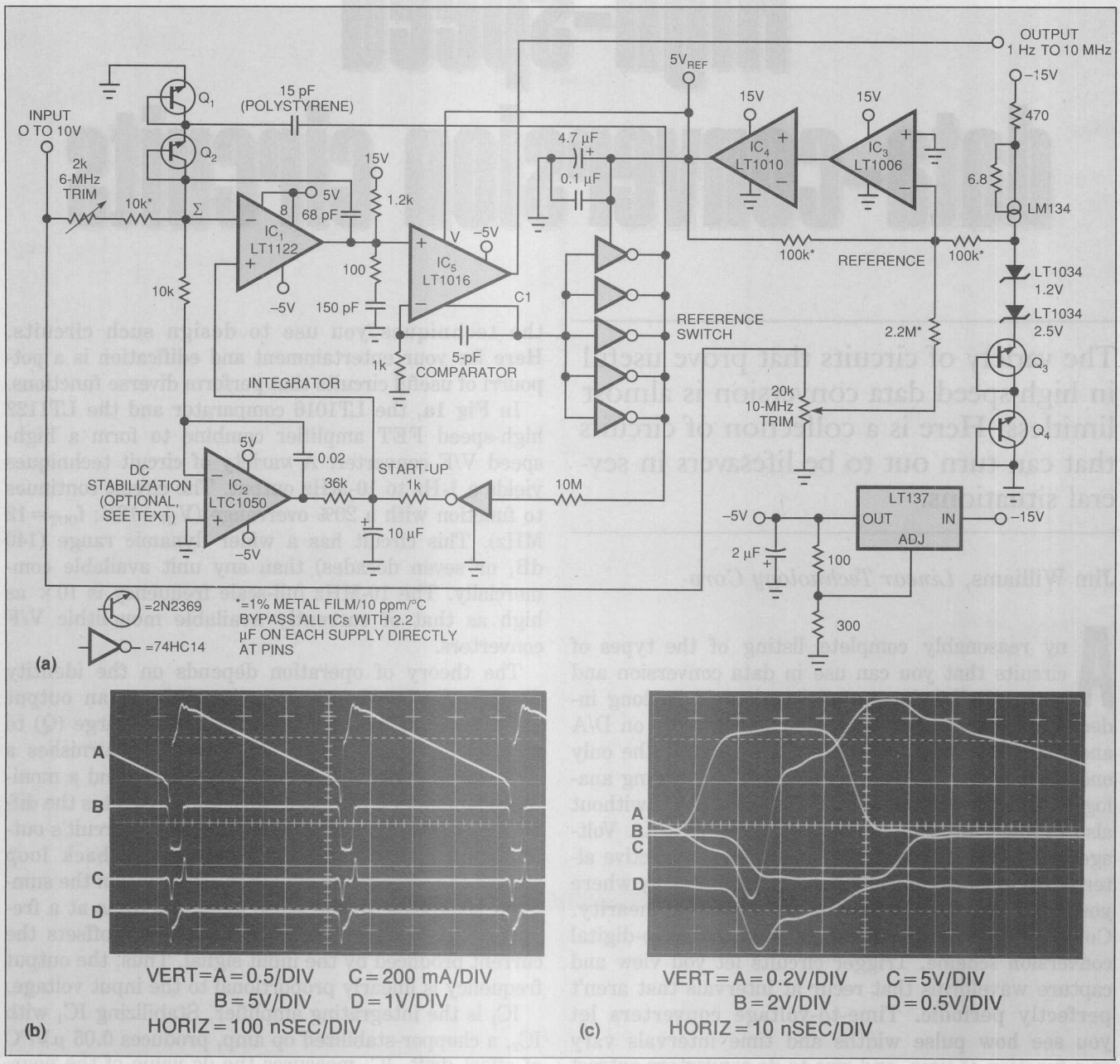


Fig 1—A voltage-to-frequency converter *with a maximum output frequency of 10 MHz and a 140-dB dynamic range is only moderately complex (**a**). In **b**, you see the circuit waveforms; **c** is an expanded view of the discharge-reset sequence upon which the circuit performance depends.*

IC_3 and IC_4 provide low-drift buffering and present a low-impedance reference to the supply pins of the paralleled inverters. The HCMOS outputs give essentially error-free low-resistance switching. The reference switch's output charges the 15-pF capacitor via the path that includes Q_1.

When IC_1's output crosses zero, IC_5's inverting output goes high and the reference switch (trace B) goes to ground, causing the 15-pF capacitor to dispense charge into the summing node via Q_2's base-emitter junction. The amount of charge dispensed is a direct function of the voltage that had existed across the 15-pF capacitor ($Q=CV$). Q_3 and Q_4 in the reference string provide temperature compensation for Q_1 and Q_2. The current that flows through the 15-pF capacitor (trace C) reflects the charge-pumping action. Removing current from IC_1's summing junction (trace D) drives the junction negative very quickly. The initial negative-going 15-nsec transient at IC_1's output results from amplifier delay.

The input signal feeds directly through the feedback capacitor and appears at the output. When the amplifier finally responds, its output (trace A) slew limits as the amplifier attempts to regain control of the summing node. The 1.2-kΩ pull-up resistor and the RC damper at IC_1's output enhance the amplifier's recovery from slewing. The amount of time the reference switch remains at ground depends on the 5-pF/1000Ω hysteresis network at IC_5 and on how long IC_1 takes to recover. A 60-nsec interval is long enough for the 15-pF capacitor to fully discharge. After the discharge, IC_5 changes state, the reference switch swings positive, the capacitor recharges, and the entire cycle repeats. The frequency at which this oscillation occurs is directly proportional to the current into the summing junction, and, in turn, to the input voltage. Any input current will dictate an oscillation frequency that holds the summing point at an average value of zero.

At MHz frequencies, maintaining a linear relationship between the input voltage and the output frequency places severe restrictions on the circuit timing. The key to achieving a 10-MHz full-scale operating frequency is the ability to transmit information around the loop very quickly. The discharge-reset sequence detailed in **Fig 1c** is particularly critical.

Fig 1c, trace A is the output of integrator IC_1. Its ramp output crosses zero at the first vertical graticule division on the left. A few nsec later, IC_5's inverting output begins to rise (trace B), switching the reference switch to ground (trace C). The reference switch begins to head towards ground about 16 nsec after IC_1's output crosses zero. Two nanoseconds later, the summing point (trace D) begins to go negative as current flows from it through the 15-pF capacitor. At 25 nsec, IC_5's inverting output is fully positive, the reference switch is at ground, and the summing point is at its negative extreme. Now, IC_1 begins to take control. Its output (trace A) slews rapidly in the positive direction, restoring the summing point. At 60 nsec, IC_1 is in control of the summing node and the integration ramp begins again.

Come on, get going

Start-up and overdrive conditions could force IC_1's output to go to the negative rail and stay there. The ac-coupled nature of the charge-dispensing loop can preclude normal operation and cause the circuit to latch. The remaining HCMOS inverter provides a "watchdog" function for this condition. If IC_1's output goes to the negative rail, the reference switch tries to stay at ground. The remaining inverter goes high, lifting IC_1's positive input, causing IC_1's output to slew positive, and thus initiating normal circuit action. The 1-kΩ/10-μF combination and the 10-MΩ resistor in series with the inverter input limit the loop bandwidth during start-up, preventing unwanted outputs.

The LM134 current source that drives the reference string has a built-in 0.33%/°C thermal coefficient, causing a slight voltage modulation in the Q_3/Q_4 pair over temperature. This small change (~+120 ppm/°C) opposes the −120 ppm/°C drift in the 15-pF polystyrene capacitor and reduces the temperature coefficient of the complete circuit.

Acroynms used in this article

ac—Alternating current
A/D—Analog-to-digital
ADC—Analog-to-digital converter
D/A—Digital-to-analog
DAC—Digital-to-analog converter
dc—Direct current
FET—Field-effect transistor
LSB—Least-significant bit
RC—Resistance-capacitance
rms—Root-mean-square
S/H—Sample and hold
TTL—Transistor-transistor logic
V/F—Voltage to frequency
VFC—Voltage-to-frequency converter

To trim this circuit, apply exactly 6V at the input and adjust the 2-kΩ potentiometer for 6.000-MHz output. Next, put in exactly 10V and trim the 20-kΩ potentiometer for a 10.000-MHz output. Repeat these adjustments until both points stay fixed. IC_2's low drift eliminates a zero adjustment. If operation below 600 Hz is not required, you can delete IC_2 and its associated components.

Nonlinearity of this circuit is 0.03% and full-scale drift is 50 ppm/°C. Zero-point error, controlled by IC_2, is 0.05 Hz/°C.

Fig 2a shows a simple, very fast S/H circuit. This circuit will acquire a 5V input to 8-bit accuracy in 100 nsec. The hold step amplitude is less than ¼ LSB, and hold settling time is less than 25 nsec. The aperture time is 4 nsec, and the droop rate is about ½ LSB in 1 μsec.

Inverting buffer IC_1 feeds the input to a Schottky switching bridge. The Schottky bridge, which is similar to types used in sampling oscilloscopes, switches in 1 nsec and eliminates the charge pump-through that an FET switch would contribute. The switching bridge's output feeds output-amplifier IC_2. IC_2, configured as

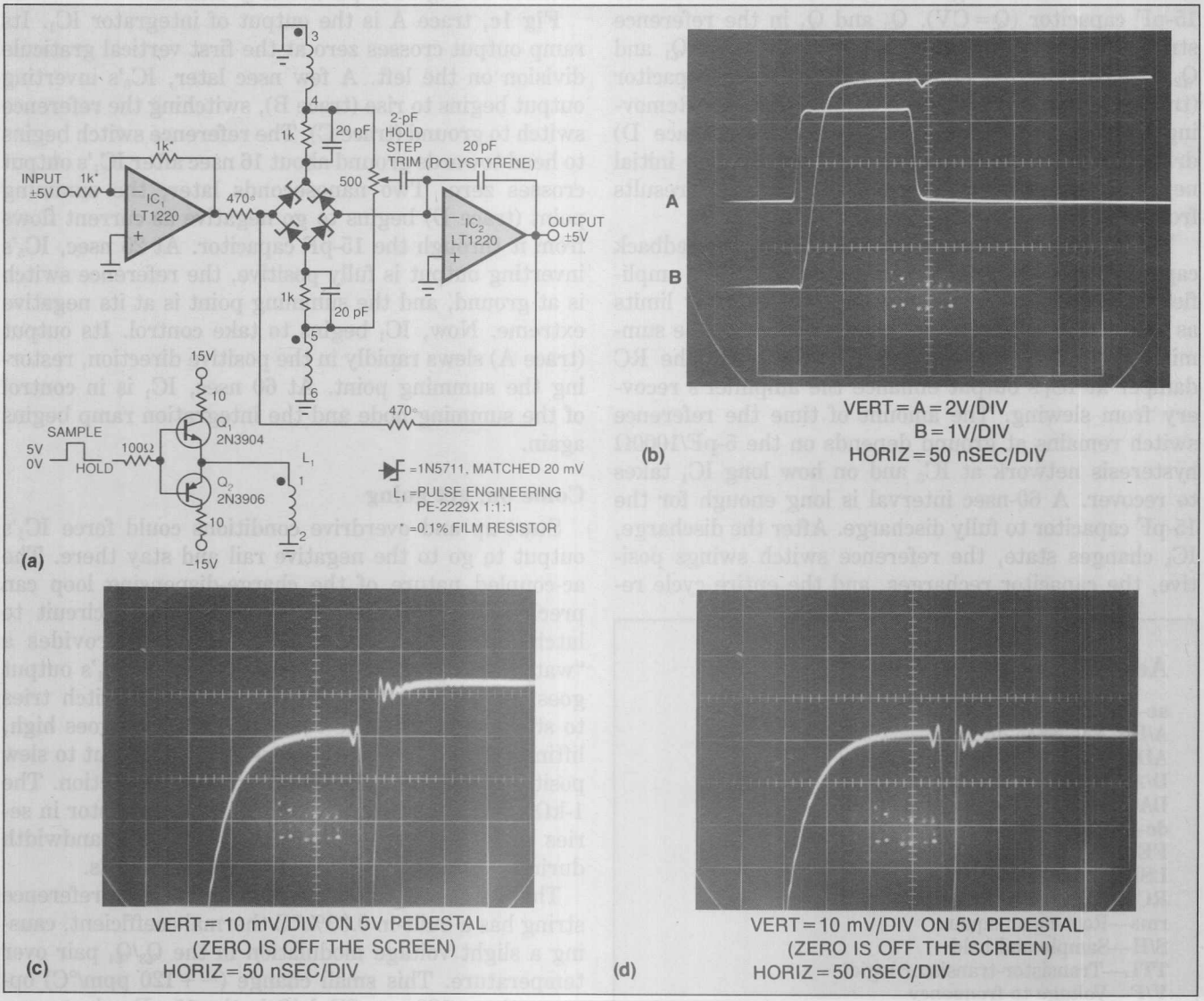


Fig 2—This very fast S/H circuit (a), *acquires signals to 8-bit accuracy in 100 nsec. In* ***b*** *you see the waveforms within the circuit. Accurate operation depends on cancellation of the switching signals that feed through the bridge. In* ***c****, the compensation is disconnected. In* ***d****, you can see the effect of the compensation.*

an integrator, is the actual hold amplifier. Its output feeds back to the switching bridge's input, forming a summing point with IC_1's output resistor. This feedback loop enhances accuracy by placing the bridge within a loop.

Driving the S/H input line switches the bridge. Q_1 and Q_2 drive L_1's primary. L_1's secondaries provide complementary drive to the bridge with negligible time skew.

Fig 2b shows the circuit acquiring a full-scale step. Trace A is the input command; trace B is IC_2's output. The aberration (that is, the "hold step") visible in IC_2's output when the circuit switches into the hold mode is the result of minute residual ac imbalances in the bridge. **Fig 2c** illustrates this effect in high-resolution detail, with the "hold-step trim" deliberately disconnected. After IC_2's output nominally settles at final value, the circuit switches into the hold mode. The bridge imbalance dumps a small parasitic charge into IC_2's summing point, in this case causing IC_2 to step 10 mV higher. Properly connected and adjusted, the trim supplies a small compensatory charge during switching. **Fig 2d** shows the effect of this compensation on the output. The settled hold-mode output is the same as the acquired input voltage. To trim this circuit, ground the input while pulsing the S/H control line. Next, adjust the trim for a minimal amplitude step between the S/H states.

In contrast to low-frequency S/H circuits, this circuit, if left in the sample mode, cannot pass a signal. The transformers' inherent ac coupling prevents the circuit from providing a dc output. Moreover, extending the sample-mode duration beyond 500 nsec will saturate the transformers, causing erroneous outputs and excessive dissipation in Q_1 and Q_2. If the control input can remain in the high state for extended periods, you should ac-couple the control signal.

Compare currents in 15 nsec

Fig 3a shows a way to build a high-speed current comparator with resolution in the 12-bit range. Comparing currents, which is the fastest way to compare DAC outputs with analog values, is a common technique in high-speed instrumentation, especially in high-speed A/D converters. IC_1 is a Schottky-bounded amplifier. The bounding diodes hold down the response time by preventing summing-point overdrive from causing IC_1 to saturate. Select the capacitor—it compensates for the DAC output capacitance—for the best amplifier damping; the 3-pF value shown is typical. The feedback resistor maximizes the circuit's gain-bandwidth product; the 10-kΩ value shown is also typical. Voltage gains of 4 to 10 are common.

Fig 3b shows the circuit's performance. Trace A, a test input, causes IC_1's output (trace B) to slew through zero (the screen's center horizontal line). When IC_1 crosses zero, IC_2's input goes negative and IC_2 responds 10 nsec later with a TTL output (trace C). The total time from when the test input reaches the TTL high threshold until the comparator output level becomes a TTL high is <15 nsec.

Fig 4a is an extremely versatile trigger circuit. Designing a fast, stable trigger is not easy, and often entails a considerable number of discrete components.

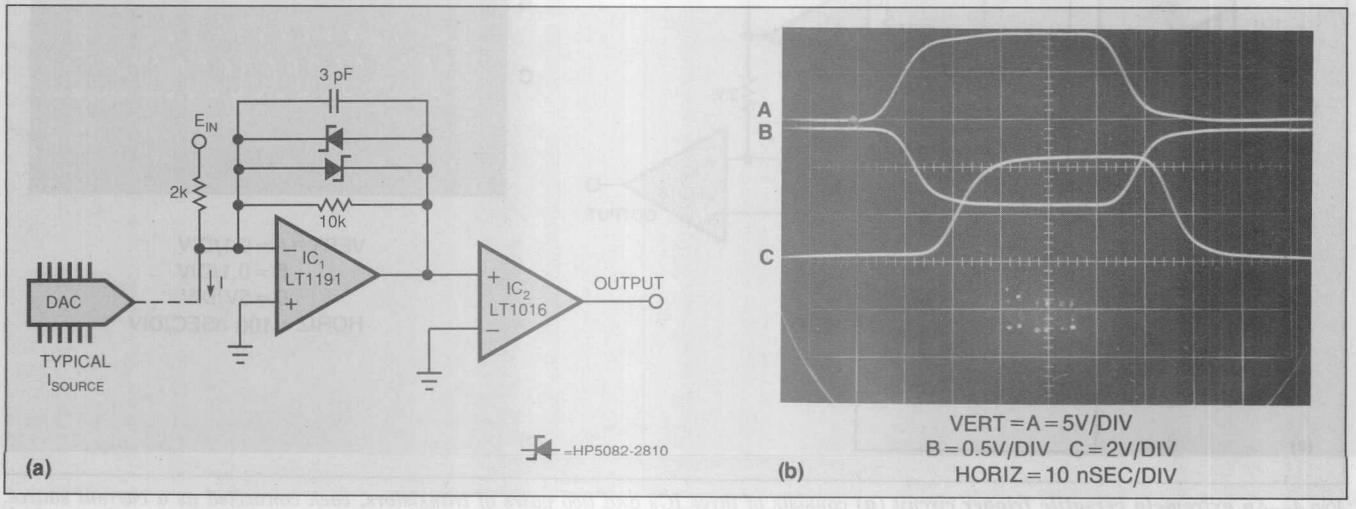


***Fig 3—Only two ICs yield a fast** summing comparator (**a**). In **b**, you can observe key waveforms as the circuit operates.*

This circuit, without level adjustment, triggers reliably from dc to 50 MHz over a 2 to 300-mV input range.

IC_1, a gain-of-10 preamplifier, feeds an adaptive trigger configuration that maintains the output comparator's (IC_3's) trip point at one-half the input-signal amplitude, regardless of the signal's magnitude. The self-adjusting trip point ensures reliable automatic triggering over a wide input-amplitude range, even for very low-level inputs. As an option, the network (shown in dashed lines in **Fig 4a**) permits changing the trip threshold. The adjustment lets you select any point on the input-waveform edge as the trigger point.

Fig 4b shows the performance for a 40-MHz input sine wave (trace A). At IC_1's output (trace B), the input signal has received voltage gain with little or no phase shift. Comparator IC_3 gives a clean logic output (trace C). At the highest frequencies, bandwidth limiting can occur in IC_1, but it is irrelevant; the adaptive trigger threshold will simply vary in proportion to the input to maintain the circuit output.

The circuit of **Fig 5a** lets you determine very short pulse widths (in this case, 250 nsec full scale) with a typical error of 1%. Digital methods of achieving similar results dictate GHz clock speeds, and thus result in cumbersome implementations. In addition, processor-based approaches that use averaging techniques require repetitive pulses; this circuit does not. Circuits of the type shown in **Fig 5a** frequently appear in automatic test equipment and nuclear and high-energy physics work, where measuring the width of short pulses is a common requirement.

The circuit functions by charging a capacitor for the duration of the pulse. When the pulse ends, the charging ceases, and the voltage across the capacitor is proportional to the width of the pulse.

The pulse whose width is to be measured (**Fig 5b**, trace A) simultaneously biases the 74C221 dual one-shot and Q_3. Q_3, aided by Baker clamping, feed-forward capacitance, and optimized dc base biasing, turns off in a few nsec. Current source Q_2's emitter becomes forward biased, and Q_2 supplies constant current to the 100-pF integrating capacitor. Q_1 supplies temperature compensation for Q_2 and the 2.5V LT1009 provides the current-source reference. The 100-pF capacitor at Q_2's collector charges in ramp fashion (trace B). IC_1 supplies a buffered output (trace C). When the input

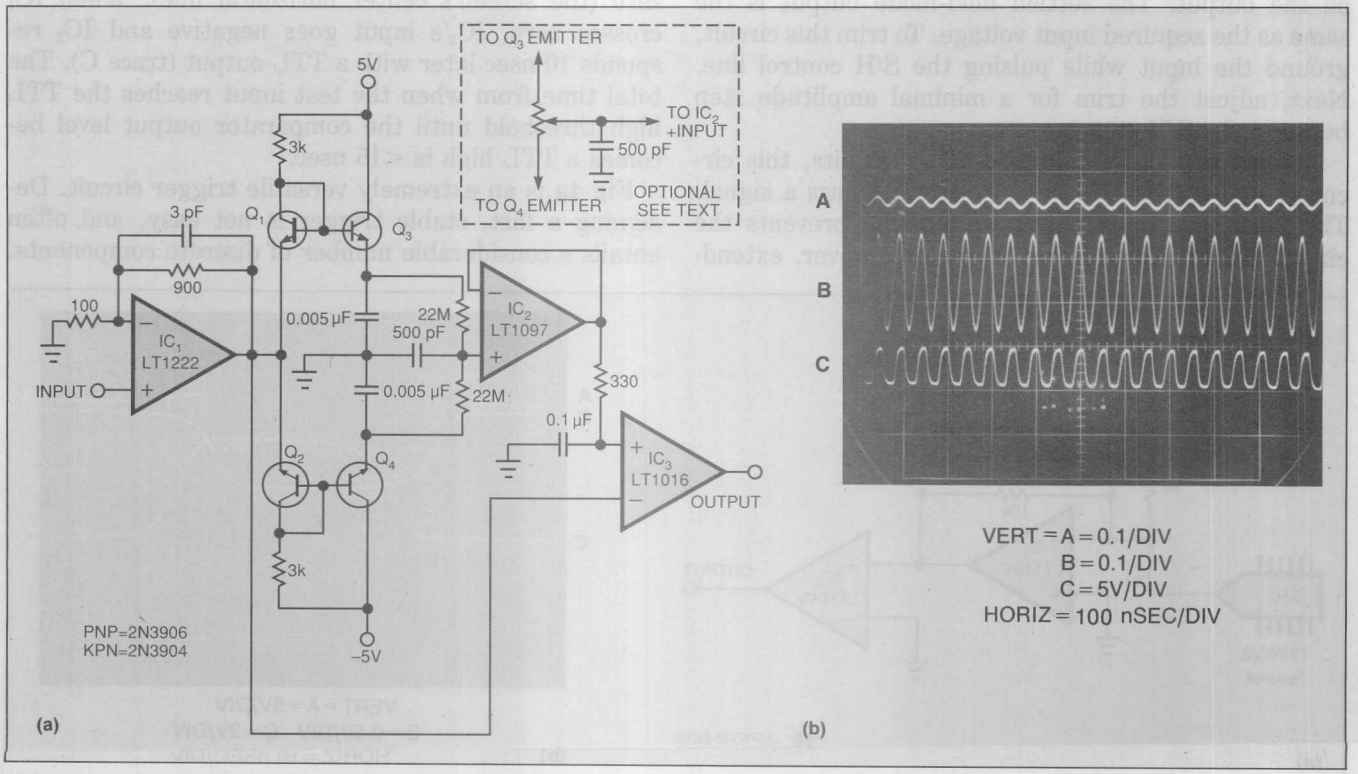


Fig 4—An extremely versatile trigger *circuit (**a**) consists of three ICs and two pairs of transistors, each connected as a current source. The circuit adjusts its threshold as the amplitude of the incoming signal varies. In **b**, you see waveforms during circuit operation.*

pulse ends, Q_3 turns on rapidly, reverse-biasing Q_2's emitter and turning off the current source. IC_1's voltage is directly proportional to the input pulse width. A monitoring A/D converter can acquire this data.

After an interval set by the 74C221's delay (a resistor and a capacitor set the delay), a pulse appears at the circuit's Q_2 output (trace D). This pulse turns on Q_4, discharging the 100-pF capacitor to zero and readying the circuit for the next input pulse.

This circuit's accuracy and resolution depend strongly on keeping the delay in switching the Q_1/Q_2 current source very short. **Fig 5c** provides amplitude and time-expanded versions of critical circuit waveforms. Trace A is the input pulse and trace B is IC_1's input, showing the beginning of the ramp's ascent. Trace C, IC_1's output, shows a delay of about 13 nsec from IC_1's input. Traces D and E, also IC_1's input and output, record similar delays introduced by IC_1 at the ramp turn-off. The photo reflects the extremely fast current-source switching; IC_1 causes most of the delay. IC_1's delay is far less critical than the current-source-switching delays. IC_1 will always settle to the correct

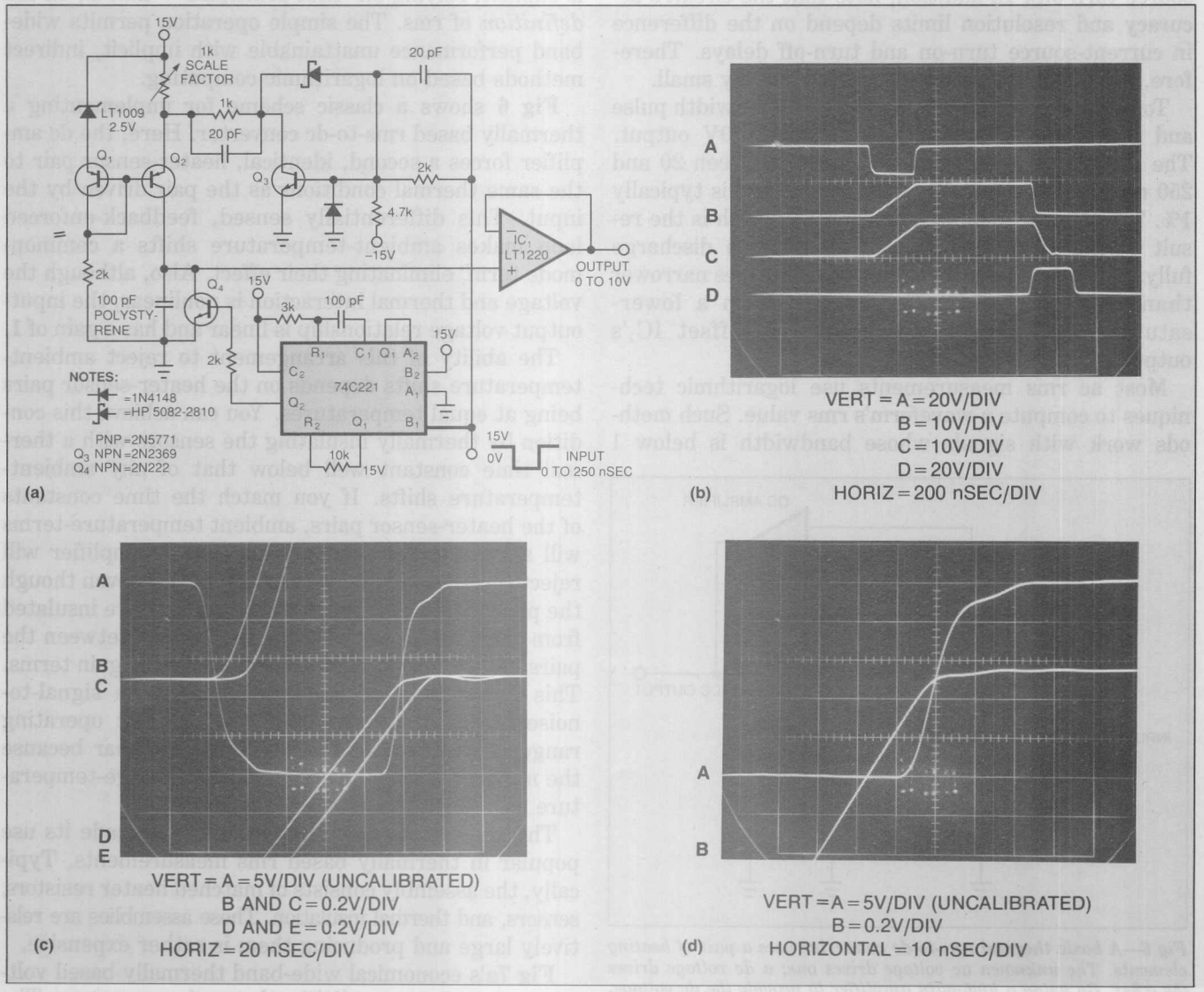


Fig 5—Changing pulse widths to voltages *provides a convenient way to monitor changes in time intervals that occur as a function of time. The circuit in* ***a*** *performs this function. In* ***b*** *you see circuit waveforms. These waveforms appear in expanded form in* ***c****. The current-source turn-off appears in* ***d****.*

value well before the one-shot resets the circuit. In practice, you should not trigger a monitoring A/D converter until about 50 nsec after the circuit's input pulse has ceased. This delay gives IC_1 plenty of time to catch up to the 100-pF capacitor's settled value.

As mentioned, fast current-source switching is essential for good results. **Fig 5d** details the current-source turn-off. Trace A is the circuit's input-pulse rising edge, and trace B shows the "top" of the ramp. Turn-off occurs in a few nanoseconds. Similar speed is characteristic of the input's falling edge (current-source turn-on). In addition, note that the circuit's accuracy and resolution limits depend on the difference in current-source turn-on and turn-off delays. Therefore, the effective overall delay is extremely small.

To calibrate this circuit, apply a 250-nsec-width pulse and trim the 1-kΩ potentiometer for a 10V output. The circuit will convert pulse widths between 20 and 250 nsec to voltages with an accuracy that is typically 1%. The 20-nsec minimum-measurable width is the result of the 100-pF capacitor's inability to discharge fully. If you must measure the width of pulses narrower than 20 nsec, you can replace Q_4 with a lower-saturation-voltage device or you can offset IC_1's output.

Most ac rms measurements use logarithmic techniques to compute a waveform's rms value. Such methods work with signals whose bandwidth is below 1 MHz and whose crest factor is less than about 10. Practically speaking, a waveform's ability to heat a resistive load defines its rms value. Specialized instruments employ thermally based assemblies that compute the rms values of input signals. Compared with logarithmically based converters, thermal methods work over a substantially wider bandwidth and produce accurate results with signals that have much higher crest factors (ratio of peak to rms voltage).

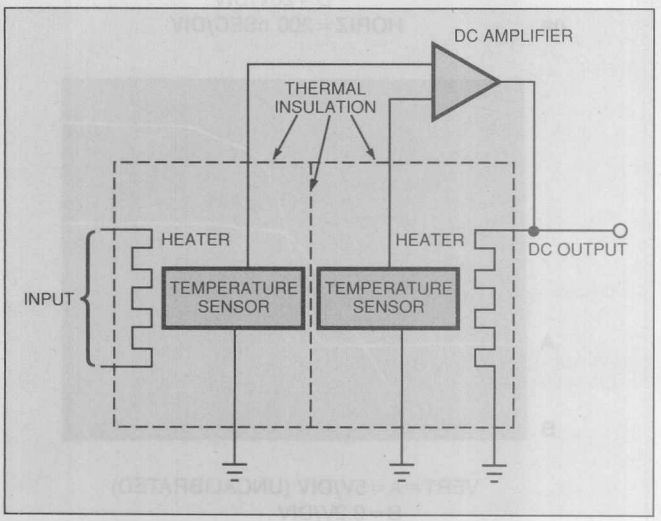


***Fig 6—A basic thermal rms-to-dc converter** uses a pair of heating elements. The unknown ac voltage drives one; a dc voltage drives the other. By using a high-gain amplifier to provide the dc voltage, you force the heating effect of the dc to equal that of the ac. Hence the rms value of the dc and ac are equal. Thus, when you measure the dc voltage, you are measuring the rms ac voltage.*

Thermal rms-to-dc converters are direct acting, thermoelectronic analog computers. The thermal technique is explicit, relying on "first principles"—that is, on the *definition* of rms. The simple operation permits wideband performance unattainable with implicit, indirect methods based on logarithmic computing.

Fig 6 shows a classic scheme for implementing a thermally based rms-to-dc converter. Here, the dc amplifier forces a second, identical, heater-sensor pair to the same thermal conditions as the pair driven by the input. This differentially sensed, feedback-enforced loop makes ambient-temperature shifts a common-mode term, eliminating their effect. Also, although the voltage and thermal interaction is nonlinear, the input-output voltage relationship is linear and has a gain of 1.

The ability of this arrangement to reject ambient-temperature shifts depends on the heater-sensor pairs being at equal temperatures. You can achieve this condition by thermally insulating the sensors with a thermal time constant well below that of any ambient-temperature shifts. If you match the time constants of the heater-sensor pairs, ambient temperature-terms will affect the pairs equally and the dc amplifier will reject this common-mode term. Note that, even though the pairs are at equal temperatures, they are insulated from each other. Any thermal interaction between the pairs reduces the system's thermally based gain terms. This interaction would cause unfavorable signal-to-noise performance and limit the dynamic operating range. The output of **Fig 6**'s circuit is linear because the matched thermal pairs' nonlinear voltage-temperature relationships cancel each other.

The advantages of this approach have made its use popular in thermally based rms measurements. Typically, the assembly consists of matched heater resistors, sensors, and thermal insulation. These assemblies are relatively large and producing them is rather expensive.

Fig 7a's economical wide-band thermally based voltmeter uses a monolithic thermal converter. The LT1223 amplifier provides gain and drives the LT1088 rms-to-dc thermal converter. The supply biases the

LT1088's temperature-sensing diodes. IC_1, set up as a differential servo amplifier with a gain of 9000, extracts the diode's difference signal and biases Q_1. Q_1 drives one of the LT1088's heaters, completing a loop. The 3300-pF capacitor gives a stable roll-off. The 1.5-MΩ/0.0225-μF combination improves settling by reducing the gain during output slewing. The LT1088's square-law thermal gain makes the overall loop gain lower for small inputs. Normally, the low gain would cause slow settling for values below about 10 to 20% of full scale. The LT1004 1-kΩ/3-kΩ network provides a simple breakpoint that boosts the amplifier gain at low signal levels to improve settling. IC_2, a gain-trimmable output stage, compensates for gain variations in the two sides of the LT1088.

To trim the circuit, apply a dc signal of about 10% of full scale (that is, 0.05V) and adjust the "zero trim" so that $V_{OUT} = V_{IN}$. Next, apply a full-scale dc input and set the full-scale trim for a full-scale output. Repeat the trims until both errors are well below 1% of full-scale. An alternate trimming scheme involves applying no input, grounding Q_1's base, and adjusting the zero trim until IC_1's output is active. Then you disconnect Q_1's base from ground, apply a full-scale input, and trim the full-scale adjustment to produce a full-scale output.

Fig 7b is a plot of the circuit's error vs input fre-

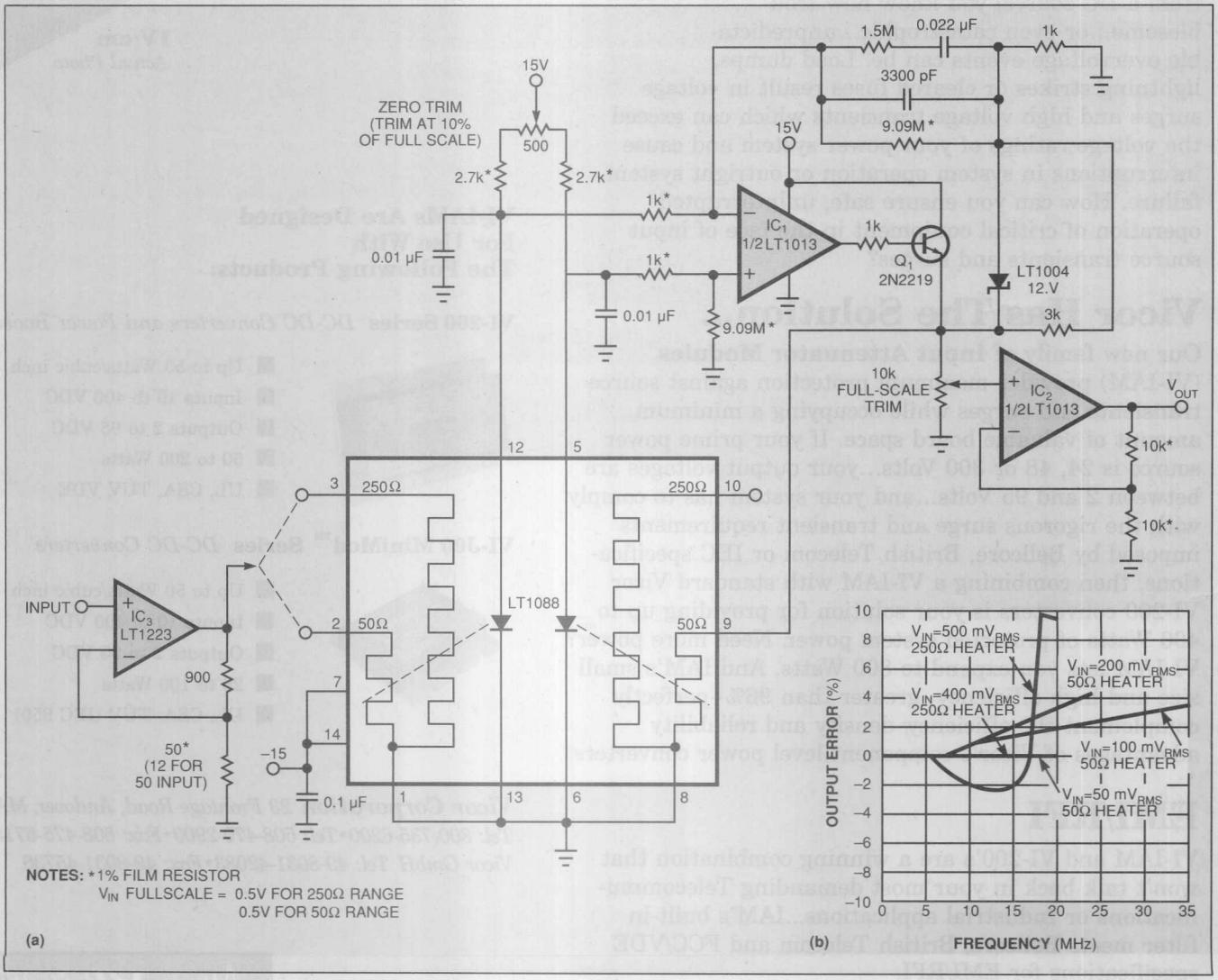
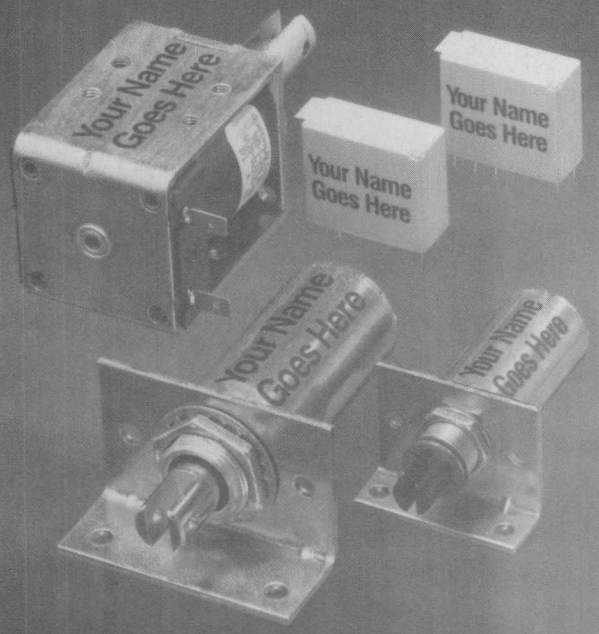


***Fig 7—A functioning rms-to-dc converter** appears in **a**. In **b**, you see the circuit's error vs frequency for several input-signal amplitudes and for two values of heater resistance.*

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quency. When you apply your input to one of the 50Ω heaters, the LT1088's error spec is 2% to 100 MHz; using a 250Ω heater, the spec is 1% to 20 MHz. Most of the error shown results from bandwidth restrictions in IC_3, but the performance is still impressive. The plots include data taken at various input levels into both a high and a low-resistance heater. The error in the response to a 500-mV input into the 250Ω heater rises to 1% at 8 MHz, and 2.5% at 14 MHz before peaking badly beyond 17 MHz. This input level forces a 9.5V-rms output at IC_3, and introduces large-signal bandwidth limitations. The 400-mV input to the 250Ω heater produces essentially flat response to 20 MHz, the LT1088's 250Ω-heater specification limit.

The 50Ω heater provides significantly wider bandwidth, although in the circuit of **Fig 7a**, IC_3's 50-mA output limits the maximum input to about 100-mV rms (1.76V rms at the LT1088).

As you can see, the circuits discussed here are useful in their own right. They are also thought provoking. You can combine and modify them virtually without limit, and in so doing, produce new circuits that perform many other useful functions. EDN

Author's biography

For more information on this article's author, turn to pg 163 in the October 10, 1991 issue.

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